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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/584,620	06/26/2006	Eiichi Sadayuki	28951.1179	8160
53067 7590 03/02/2009 STEP TOE & JOHNSON LLP 1330 CONNECTICUT AVE., NW WASHINGTON, DC 20036				
EXAMINER				
WILLIAMS, ARUN C				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/584,620

Applicant(s)

SADAYUKI ET AL.

Examiner

ARUN WILLIAMS

Art Unit

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/2/2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) 9-12 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7 and 8 is/are allowed.
- 6) ☒ Claim(s) 1-3, 5, and 6 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 6/26/2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

This is in response to an amendment/response filed on 12/2/2008

Claims 1-8 have been amended.

Claims 9-12 have been cancelled.

No new claims added.

Hereon claims 1-8 are currently pending wherein claims 1-3,5,6 are rejected, claim 4 is objected, and claims 7 and 8 are allowed.

Response to Arguments

Applicant's arguments filed 12/2/2008 have been fully considered but are now moot in view of the new grounds of rejection necessitated by amendment.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable by Murayama et al, (Murayama), USPATNO.(6,118,295) in view of Ozeki et al, (Ozeki), USNO.(2005/0146378)

As for claim 1, Murayama discloses and shows in Fig. 1 a semiconductor device comprising: a capacitance (c1) element one end of which is connected to a power supply (Vdd); a first comparator(11) which has two input nodes having opposite polarity to each other, a first input node of the two input nodes for receiving a reference voltage (VA) and a second input node of the two input nodes connected to an output of the other end of the capacitance element at their inputs to compare the respective voltage values to output a first output signal indicating a comparison result; a first resistor (R1) element which connects the first input node and the second input node of the first comparator; wherein the first comparator activates the output signal indicating the comparison result when the voltage difference between the inputted_reference voltage

and the inputted output of the other end of the capacitance element occurs power supply voltage varies(col.2-3, lines 66-16).

Murayama differs from the claimed invention because he does not explicitly disclose the capacitance element for detecting a voltage variation of the power supply.

Ozeki discloses the capacitance (Cs) element for detecting a voltage variation of the power supply (Vdd) (par.[0085]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Murayama by using the capacitance element for detecting a voltage variation of the power supply for advantages such as providing the ability to detect potential power supply line changes (par.[0085]), as taught by Ozeki.

As for claim 3, Murayama shows in Fig. 1 a second (R2) resistor element having a first end directly connected to said power supply; a third resistor element (R3) element having a first end connected to a second end of the second resistor (R2) and having a second end directly connected to a ground terminal; a second comparator (12) having two input nodes directly connected to the first end of the third resistor element and the reference voltage terminal, respectively, and for outputting a second output signal indicating a second comparison result; and a logic OR circuit (13) which performs a logic OR operation of the first output signal of the first comparator and the second output signal of the second comparator.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama in view of Ozeki and further in view of Dancy et al,(Dancy), USPATNO.(6,577,109).

As for claim 2, Murayama in view of Ozeki discloses all limitations, but differs from the claimed invention because he does not explicitly disclose a hysteresis comparator which outputs the first output signal indicating the first comparison result when the voltage difference between the inputted reference voltage and the output of the other end of the capacitance element becomes larger than a predetermined hysteresis width.

Dancy discloses and shows in Fig. 9 a hysteresis comparator (901) which outputs the first output signal indicating the first comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis width (col.10, lines 12-23).

Dancy is evidence that ordinary skill in the art would find a reason, suggestion or motivation to use a hysteresis comparator which activates the output signal indicating the comparison result when the voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis width.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Murayama modified by Ozeki by a hysteresis comparator which activates the output signal indicating the comparison result when the

voltage difference between the inputted reference voltage and the inputted output of the other end of the capacitance element becomes larger than a predetermined hysteresis width for advantages such as providing the ability of an adjustable comparator (col. 10, lines 12-23), as taught by Dancy.

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama in view of Ozeki and further in view of Massie et al, (Massie), USPATNO.(6,271,650).

As for claims 5 and 6, Murayama in view of Ozeki discloses all limitation, but differs from the claimed invention because he does not explicitly disclose a switching part for switching a value of the output of the other end of the capacitor element to an arbitrary value and a control section which operates the switching part at turning on the power of the semiconductor device.

Massie discloses and shows in Fig. 3 a switching part (307) for switching a value of the output of the other end of the capacitor element (311) to an arbitrary value (col. 5, lines 48-63). Furthermore, Massie discloses and shows in Fig. 3 and a control section (305) which operates the switching part at turning on the power of the semiconductor device (col. 6, lines 7-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Murayama modified by Ozeki by using a switching part for switching a value of the output of the other end of the capacitor element to an arbitrary value and a control section which operates the switching part at

turning on the power of the semiconductor device advantages such as providing the cyclical control of the output (col.6, line 8-9), as taught by Massie.

Allowable Subject Matter

7. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. Claims 7 and 8 are allowed over the prior art as of record.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ARUN WILLIAMS whose telephone number is (571)272-9765. The examiner can normally be reached on Mon - Thurs, 6:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on 571-272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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